Notice of Allowability	Application No.	Applicant(s)	
	09/730,039	MOHAMED ET AL.	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *19 May 2006*.

2. ☒ The allowed claim(s) is/are *29-46 renumbered as 1-18*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. Authorization for this examiner's amendment was given in a telephone interview with Michael Farjami, Esq. (Reg. No. 38,185) on 31 July 2006. All amendments have been bolded, underlines are added language and strikethroughs are deleted language.

3. The application has been amended as follows:

a. Claim 29: A processor comprising:

i. A first thread and a second thread, said first thread comprising a first processing unit and said second thread comprising a second processing unit;

ii. A first instruction packet and a second instruction packet, said first instruction packet comprising at most two issue groups and said second instruction packet comprising at most two issue groups, each of said at most two issue groups of said first instruction packet and each of said at most two issue groups of said second instruction packet comprising at most 64 bits and ~~**requiring**~~ an internal instruction bus no greater than 64 bits wide for transport to one of said first and second processing units;

iii. Each of said first and second threads receiving a respective one of said at most two issue groups of a respective one of said first and second instruction packets;

iv. Said first processing unit executing one of said at least two issue groups of said first instruction packet and said second processing unit executing one of said at most two issue groups of said second instruction packet in a single clock cycle;

v. Each of said at most two issue groups of each of said first and second instruction packets performing an operation on data fetched from an exclusive thread memory communicating with only one of said first and second threads, a result of said operation being stored back in said exclusive thread memory communicating with said only one of said first and second threads.

b. Claim 40: A method for improving performance of a VLIW processor comprising:

i. Dividing a first instruction packet into first and second issue groups and a second instruction packet into first and second issue groups, each of said first and second issue groups of said first instruction packet and said first and second issue groups of said second instruction packet comprising at most 64 bits;

ii. Providing each of said first and second issue groups of said first instruction packet and said first and second issue groups of said second

instruction packet, in one of two clock cycles, to a respective thread having a respective processing unit, ~~said each of said first and second issue groups of said first instruction packet and said first and second issue groups of said second instruction packet requiring~~ and an internal instruction bus no greater than 64 bits wide for transport to said respective processing unit;

iii. Executing said first and second instruction packets in said two clock cycles, wherein an issue group from each of said first and second instruction packets is executed in one of said two clock cycles;

iv. Fetching data from an exclusive thread memory communicating with only one thread;

v. Performing an operation on said data by one of said first and second issue groups of said first instruction packet and said first and second issue groups of said second instruction packet;

vi. Storing back a result of said operation in said exclusive thread memory communicating with said only one thread.

4. The following is an examiner's statement of reasons for allowance: The independent claims, taking claim 1 as example, comprise the limitations of two instruction packets with, at most, two issue groups, therefore limiting his invention to a system with, at most, two issue groups in a packet. The claim further limits itself by stating that each issue group is at most 64 bits and an issue group from each packet is executed by an associated processing unit with the thread the respective instruction packet in a single cycle. The claim also limits itself to a bus of

at most 64 bits to transport the issue groups to their respective processing units. The prior art searched and found does not explicitly the instruction packets to two issue groups, issuing one issue group from multiple instruction packets to associated processing units in a single cycle, and a bus of at most 64 bits. The prior art references for very long instruction words with at most four issue groups and limited size to the issue groups executing within a singly threaded system, so they did not have the multiple processing units associated with individual threads nor teach the internal instruction bus of no greater than 64 bits. The prior art references that did teach multiple processing units and shared memory did not teach the specifics on the very long instruction words nor the internal instruction bus of no greater than 64 bits. Also, there is no reason to combine the references.

5. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:00am-4:30pm.

7. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

8. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AJL
Aimee J. Li
31 July 2006

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